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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,105	06/22/2001	Michael Ruehle	2207/11839	7951

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,105	RUEHLE, MICHAEL	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-10, 19-20, 29-30 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 9, 19 and 29 recite the limitation "the plurality of second memory devices" in Line 2 of the respective claims. There is insufficient antecedent basis for this limitation in the claim.

4. Claims 10, 20, and 30 are rejected because it depends on the rejected claims 9, 19, and 29, respectively.

5. Claim 34 recites the limitation "the plurality of second devices" in Line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7, 9-17, 19-27, 29-34, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Dent et al('575), hereinafter referred to as Dent.

8. Regarding claim 1, Dent discloses a system to initiate, by a host(Figure 1, 5), an event in a first device(Figure 2, Combination of Components 20, 24, 25, 34), the system comprising: a signal line(Figure 2, DATA/ADDR BUS, Read, Write, M1) to communicate a plurality of data values between a host and

one or more second devices(Figure 2, 7); and a tap line to communicate said plurality of data values between said signal line and said first device; wherein said event is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 6, Lines 10-17), and wherein said event selectively switches a communication path from a third device(Figure 2, 8) to one of said host and said first device(Column 6, Lines 10-17; Column 10, Lines 41-46; Either the third device is connected to the host or the coprocessor of the first device).

9. Regarding claim 2, Dent discloses switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

10. Regarding claim 3, Dent discloses switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

11. Regarding claim 4, Dent discloses wherein the host is a processor(Figure 1, 5).

12. Regarding claim 5, Dent discloses the first device is a logic device(Figure 2, Combination of Components 20, 24, 25, 34; The device performs logic and therefore is a logic device).

13. Regarding claim 6, Dent discloses the second device being a memory device(Figure 2, 7).

14. Regarding claim 7, Dent discloses the third device being a memory device(Figure 1, 8).

15. Regarding claim 9 as best understood, Dent discloses the plurality of data values representing a memory location within the second memory device(Figure 2; Data values on the Address bus represents the memory location in the second device).

16. Regarding claim 10, Dent discloses the utilization of a data value provides a call to the represented memory location(Figure 2; Data values on the Address bus represents the memory location in the second device, and results in an call to that location).

17. Regarding claim 11, Dent discloses a method to initiate, by a host(Figure 1, 5), an event in a first device(Figure 2, Combination of Components 20, 24, 25, 34) comprising: communicating, by a signal line(Figure 2, DATA/ADDR BUS, Read, Write, M1), a plurality of data values between a host and one or more second devices(Figure 2, 7); communicating by a tap line, said plurality of data values between said signal line and said first device; initiating said event upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 6, Lines 10-17), and selectively switching a communication path from a third device(Figure 2, 8) to one of said host and said first device(Column 6, Lines 10-17; Column 10, Lines 41-46; Either the third device is connected to the host or the coprocessor of the first device).

18. Regarding claim 12, Dent discloses a method, wherein the event comprises a switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

19. Regarding claim 13, Dent discloses a method, wherein the event comprises a switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

20. Regarding claim 14, Dent discloses the host is a processor(Figure 1, 5).

21. Regarding claim 15, Dent discloses the first device is a logic device(Figure 2, Combination of Components 20, 24, 25, 34; The device performs logic operations and therefore is a logic device).

22. Regarding claim 16, Dent discloses the second device being a memory device(Figure 2, 7).

23. Regarding claim 17, Dent discloses the third device being a memory device(Figure 1, 8).

24. Regarding claim 19, as best understood, Dent discloses the plurality of data values representing a memory location within the second memory device(Figure 2; Data values on the Address bus represents the memory location in the second device).

25. Regarding claim 20, Dent discloses the utilization of a data value provides a call to the represented memory location(Figure 2; Data values on the Address bus represents the memory location in the second device, and results in an call to that location).

26. Regarding claim 21, Dent discloses a set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to initiate, by a host(Figure 1, 5), an event in a first device(Figure 2, Combination of Components 20, 24, 25, 34) comprising: communicating, by a signal line(Figure 2, DATA/ADDR BUS, Read, Write, M1), a plurality of data values between a host and one or more second devices(Figure 2, 7); communicating by a tap line, said plurality of data values between said signal line and said first device; initiating said event upon detection, by said first device, of a predetermined sequence of data values on the tap line(Column 6, Lines 10-17), and selectively switching a communication path from a third device(Figure 2, 8) to one of said host and said first device, in response to said detection(Column 6, Lines 10-17; Column 10, Lines 41-46; Either the third device is connected to the host or the coprocessor of the first device).

27. Regarding claim 22, Dent discloses a method, wherein the event comprises a switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

28. Regarding claim 23, Dent discloses a method, wherein the event comprises a switching of the communication path between the first device and the third device and a communication path between the signal line and the third device(Column 6, Lines 10-17; Column 10, Lines 41-46).

29. Regarding claim 24, Dent discloses the host is a processor(Figure 1, 5).

30. Regarding claim 25, Dent discloses the first device is a logic device(Figure 2, Combination of Components 20, 24, 25, 34; The device performs logic operations and therefore is a logic device).

31. Regarding claim 26, Dent discloses the second device being a memory device(Figure 2, 7).

32. Regarding claim 27, Dent discloses the third device being a memory device(Figure 1, 8).

33. Regarding claim 29, as best understood, Dent discloses the plurality of data values representing a memory location within the second memory device(Figure 2; Data values on the Address bus represents the memory location in the second device).

34. Regarding claim 30, Dent discloses the utilization of a data value provides a call to the represented memory location(Figure 2; Data values on the Address bus represents the memory location in the second device, and results in an call to that location).

35. Regarding claim 31, Dent discloses a system comprising a first device(Figure 2, Combination of Components 20, 24, 25, 34) to execute a variety of computationally intensive tasks(Column 10, Lines 41-46); a memory bus(Figure 2, DATA/ADDR BUS, Read, Write, M1) to communicate a plurality of data values between a host and one or more second devices(Figure 2, 7); a tap line to communicate said plurality of data values between the memory bus and the first device; and a memory device(Figure 2, 7) selectively coupled, by a bus switch line(Figure 2, 23) and the memory bus, to one of the host and first device, wherein the bus switch line is coupled with the memory device and the bus switch line is selectively switched between the first device and the host in response to an event initiation(Column 6, Lines 10-17; Column 10, Lines 41-46; Either the memory device is connected to the host or the coprocessor of the first device).

36. Regarding claim 32, Dent discloses a system, wherein the tap line communicatively connects the first device with the host via the memory bus(Figure 2), and wherein a sequence of control signals sent from the host to the first device cause an event initiation(Column 6, Lines 10-17).

37. Regarding claim 33, Dent discloses a system, wherein the sequence of control signals comprise a sequence of address locations(Column 6, Lines 10-17).

38. Regarding claim 34, as best understood, Dent discloses a system, wherein the one or more second devices comprise memory devices(Figure 2, 7), and wherein the address locations represent memory

locations within any of the plurality of second devices(Figure 2; Data values on the Address bus represents the memory location in the second device).

39. Regarding claim 38, Dent discloses a system, wherein, wherein an event initiation is to be controlled by the host and the selective switching of the bus switch is to be controlled by the first device(Column 12, Lines 31-39).

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 8, 18, 28, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dent, in view of what is well known in the art.

42. Regarding claim 8, Dent discloses the host is a microprocessor chipset(Figure 1, 5) and the third device is Synchronous Dynamic Random Access Memory(SDRAM)(Figure 2, 8; SDRAM is a form of RAM). Dent does not specifically disclose the first device is a Field Programmable Gate Array (FPGA) or that each of the one or more second devices is a Dual In-line Memory Module (DIMM). However, Official Notice is being taken that FPGAs are commonly used in the industry for their flexibility in programming, as exemplified by the "FPGA/ASIC selection" reference submitted with applicant's remarks. Therefore it would have been obvious to use an FPGA for the first device, since this would allow the functionality of the device to be changed if a need arises. Also, Official Notice is being taken that DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Dent's invention.

43. Regarding claim 18, Dent discloses the host is a microprocessor chipset(Figure 1, 5) and the third device is Synchronous Dynamic Random Access Memory(SDRAM)(Figure 2, 8; SDRAM is a form of RAM). Dent does not specifically disclose the first device is a Field Programmable Gate Array (FPGA) or that each of the one or more second devices is a Dual In-line Memory Module (DIMM). However, Official Notice is being taken that FPGAs are commonly used in the industry for their flexibility in programming, as exemplified by the "FPGA/ASIC selection" reference submitted with applicant's remarks. Therefore it would have been obvious to use an FPGA for the first device, since this would allow the functionality of the device to be changed if a need arises. Also, Official Notice is being taken that DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Dent's invention.

44. Regarding claim 28, Dent discloses the host is a microprocessor chipset(Figure 1, 5) and the third device is Synchronous Dynamic Random Access Memory(SDRAM)(Figure 2, 8; SDRAM is a form of RAM). Dent does not specifically disclose the first device is a Field Programmable Gate Array (FPGA) or that each of the one or more second devices is a Dual In-line Memory Module (DIMM). However, Official Notice is being taken that FPGAs are commonly used in the industry for their flexibility in programming, as exemplified by the "FPGA/ASIC selection" reference submitted with applicant's remarks. Therefore it would have been obvious to use an FPGA for the first device, since this would allow the functionality of the device to be changed if a need arises. Also, Official Notice is being taken that DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Dent's invention.

45. Regarding claim 35, Dent does not specifically disclose the first device is a Field Programmable Gate Array (FPGA). However, Official Notice is being taken that FPGAs are commonly used in the

industry for their flexibility in programming, as exemplified by the "FPGA/ASIC selection" reference submitted with applicant's remarks. Therefore it would have been obvious to use an FPGA for the first device, since this would allow the functionality of the device to be changed if a need arises.

46. Regarding claim 36, Dent discloses a system, wherein the memory device is Synchronous Dynamic Random Access Memory(SDRAM)(Figure 2, 8; SDRAM is a form of RAM).

47. Regarding claim 37, Dent does not specifically disclose that the one or more second devices comprises one or more Dual In-line Memory Modules(DIMMs). However, Official Notice is being taken that DIMMs have become an industry standard because it can be installed one at a time compared to SIMMs requirement of being installed in pairs. Therefore, it would have been obvious to use DIMMs in Dent's invention.

Response to Arguments

48. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

49. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
September 16, 2004

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